AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A semiconductor device, comprising:

a thin film transistor including a semiconductor layer that includes a channel region~~;~~, a source region, and a drain region;

a gate insulating film provided on the semiconductor layer; and

a gate electrode for controlling a conductivity of the channel region; wherein

the gate electrode includes an inclined side surface;

a surface of the semiconductor layer includes a protruding portion located under the inclined side surface of the gate electrode;

a cross-section of the gate electrode includes first and second opposing sides that are parallel to each other and a third side that is not parallel to any other side of the cross-section of the gate electrode; and

a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer.

Claim 2 (original): A semiconductor device, comprising a thin film transistor including a semiconductor layer that includes a channel region, a source region and a drain region, a gate insulating film provided on the semiconductor layer, and a gate electrode for controlling a conductivity of the channel region, wherein the semiconductor layer includes a protruding portion, a cross-sectional shape of the gate electrode includes a first step portion and a second step portion provided on the first step portion, and a side surface inclination angle of each of the first and second step portions is larger than an inclination angle of the protruding portion of the semiconductor layer.

Claim 3 (original): The semiconductor device according to claim 2, wherein the gate electrode includes a first conductive film provided on the gate insulating film and a second conductive film provided on the first conductive film, a width of the first conductive film is larger than that of the second conductive film, and the first and second conductive films form the first and second step portions, respectively.

Claim 4 (previously presented): The semiconductor device according to claim 1, wherein a surface of the semiconductor layer includes a plurality of protruding portions, and the side surface inclination angle of the gate electrode is larger than an inclination angle of any of the plurality of protruding portions of the semiconductor layer.

Claim 5 (previously presented): The semiconductor device according to claim 2, wherein a surface of the semiconductor layer includes a plurality of protruding portions, the side surface inclination of each of the first and second step portions of the gate electrode is larger than an inclination angle of any of the plurality of protruding portions of the semiconductor layer.

Claim 6 (previously presented): The semiconductor device according to claim 1, wherein the side surface inclination angle of the gate electrode is about 75° to about 90°.

Claim 7 (previously presented): The semiconductor device according to claim 2, wherein the side surface inclination of each of the first and second step portions of the gate electrode is about 75° to about 90°.

Claim 8 (previously presented): The semiconductor device according to claim 1, wherein the inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°.

Claim 9 (previously presented): The semiconductor device according to claim 2,

wherein the inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°.

Claim 10 (original): The semiconductor device according to claim 1, wherein an average height of the protruding portion is about 8 nm to about 60 nm.

Claim 11 (original): The semiconductor device according to claim 2, wherein an average height of the protruding portion is about 8 nm to about 60 nm.

Claim 12 (original): The semiconductor device according to claim 1, wherein an average surface roughness of a surface of the semiconductor layer is about 4 nm to about 30 nm.

Claim 13 (original): The semiconductor device according to claim 2, wherein an average surface roughness of a surface of the semiconductor layer is about 4 nm to about 30 nm.

Claim 14 (original): The semiconductor device according to claim 1, wherein the semiconductor layer is formed from a crystalline semiconductor film, and the protruding portion is located over a boundary between crystal grains included in the semiconductor layer.

Claim 15 (original): The semiconductor device according to claim 14, wherein the crystal grain boundary is a multipoint where three or more crystal grains meet.

Claim 16 (original): The semiconductor device according to claim 14, wherein grain diameters of the crystal grains included in the semiconductor layer are about 100 nm to about 1000 nm.

Claim 17 (canceled).

Claim 18 (original): The semiconductor device according to claim 2, wherein the semiconductor layer is formed from a crystalline semiconductor film, and the protruding portion is located over a boundary between crystal grains included in the semiconductor layer.

Claim 19 (original): The semiconductor device according to claim 18, wherein the crystal grain boundary is a multipoint where three or more crystal grains meet.

Claim 20 (original): The semiconductor device according to claim 18, wherein grain diameters of the crystal grains included in the semiconductor layer are about 100 nm to about 1000 nm.

Claim 21 (canceled).

Claim 22 (original): The semiconductor device according to claim 1, wherein the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process, and the protruding portion is formed through the melting/solidification process.

Claim 23 (original): The semiconductor device according to claim 2, wherein the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process, and the protruding portion is formed through the melting/solidification process.

Claim 24 (original): The semiconductor device according to claim 1, wherein at least a portion of the semiconductor layer includes a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

Claim 25 (original): The semiconductor device according to claim 24, wherein

the catalyst element is one or more element selected from the group consisting of nickel (Ni), iron (Fe), cobalt (Co), tin (Sn), lead (Pb), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu) and gold (Au).

Claim 26 (original): The semiconductor device according to claim 2, wherein at least a portion of the semiconductor layer includes a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

Claim 27 (original): The semiconductor device according to claim 26, wherein the catalyst element is one or more element selected from the group consisting of nickel (Ni), iron (Fe), cobalt (Co), tin (Sn), lead (Pb), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu) and gold (Au).

Claim 28 (original): The semiconductor device according to claim 1, wherein the semiconductor layer is a crystalline semiconductor film made up primarily of regions that are oriented along <111> crystal zone planes.

Claim 29 (original): The semiconductor device according to claim 28, wherein about 50% or more of the regions that are oriented along the <111> crystal zone planes are regions that are oriented along a (110) plane or a (211) plane.

Claim 30 (original): The semiconductor device according to claim 2, wherein the semiconductor layer is a crystalline semiconductor film made up primarily of regions that are oriented along <111> crystal zone planes.

Claim 31 (original): The semiconductor device according to claim 30, wherein about 50% or more of the regions that are oriented along the <111> crystal zone planes are regions that are oriented along a (110) plane or a (211) plane.

Claim 32 (original): The semiconductor device according to claim 1, wherein

domain diameters of crystal domains of the semiconductor layer are about 2 μm to about 10 μm.

Claim 33 (original): The semiconductor device according to claim 2, wherein domain diameters of crystal domains of the semiconductor layer are about 2 μm to about 10 μm.

Claim 34 (original): The semiconductor device according to claim 1, wherein a lightly-doped impurity region is provided at a junction between the channel region and the source or drain region of the semiconductor layer.

Claim 35 (original): The semiconductor device according to claim 2, wherein a lightly-doped impurity region is provided at a junction between the channel region and the source or drain region of the semiconductor layer.

Claim 36 (original): The semiconductor device according to claim 2, wherein the first step portion of the gate electrode is present in a lightly-doped impurity region.

Claim 37 (original): The semiconductor device according to claim 3, wherein the gate electrode is located above the channel region, and only the first conductive film of the gate electrode is present in a lightly-doped impurity region.

Claims 38-54 (canceled).

Claim 55 (original): An electronic device, comprising the semiconductor device according to claim 1.

Claim 56 (original): The electronic device according to claim 55, further comprising a display section where an image is displayed by using the semiconductor device.

Claim 57 (original): An electronic device, comprising the semiconductor device according to claim 2.

Claim 58 (original): The electronic device according to claim 57, further comprising a display section where an image is displayed by using the semiconductor device.

Claim 59 (new): A semiconductor device, comprising:

a thin film transistor including a semiconductor layer that includes a channel region, a source region, and a drain region;

a gate insulating film provided on the semiconductor layer; and

a gate electrode arranged to control a conductivity of the channel region; wherein

a surface of the semiconductor layer includes a protruding portion;

a cross-section of the gate electrode includes first and second opposing sides that are parallel to each other and a third side that is not parallel to any other side of the cross-section of the gate electrode;

the gate electrode has side surface inclination angles that change within a range according to the height of the gate electrode;

the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer; and

the inclination angle of the protruding portion of the semiconductor layer is about 30º to about 70º.